

In the Claims:

1-16. (Canceled)

17. (Original) An integrated circuit device, comprising:
a substrate;
an interconnection pattern having sidewalls disposed on the substrate; and
a composite insulation layer that comprises a first material layer and a second material layer disposed on the sidewalls such that the first material layer is disposed in an upper sidewall region and the second material layer is disposed in a lower sidewall region between the first material layer and the substrate, the first material layer being thicker than the second material layer.

18. (Original) An integrated circuit device as recited in Claim 17, wherein the substrate comprises a semiconductor region disposed adjacent to the interconnection pattern.

19. (Original) An integrated circuit device as recited in Claim 18, further comprising:
a conductive pad that abuts against the composite insulation layer on one of the interconnection pattern sidewalls and engages the semiconductor region.

20. (Original) An integrated circuit device as recited in Claim 17, wherein the interconnection pattern comprises:
a conductive layer; and
a cap layer disposed on the conductive layer; and wherein the integrated circuit device further comprises:
a gate insulation layer interposed between the conductive layer and the substrate.

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21. (Original) An integrated circuit device as recited in Claim 20, wherein the second material layer overlaps an interface between the conductive layer and the cap layer.

22. (Original) An integrated circuit device as recited in Claim 17, wherein the second material layer comprises a material selected from the group consisting of high density plasma (HDP) oxide, plasma-enhanced tetraethyl ortho silicate (PE-TEOS), and undoped silicate glass (USG).

23. (Original) An integrated circuit device as recited in Claim 17, wherein the first material layer comprises silicon nitride (SiN).